Please replace the abstract with the following amended abstract:

~~This invention provides a~~ In a circuit for detecting an abnormal operation of memory, an integrated circuit including the same and a method for detecting an abnormal operation, ~~capable of detecting~~ an abnormal operation of memory is detected before an error occurs in the integrated circuit of a micro-computer and the like due to [[the]] data wrongly output from the memory ~~and of~~, enhancing the reliability of the integrated circuit. More specifically, ~~this invention provides~~ a circuit is provided for detecting an abnormal operation of memory ~~comprising~~[[:]] and includes a delay circuit [[102]] for delaying an output data [[123]] of memory [[101]] for a predetermined period of time and for outputting this data as a delay data [[124]]; and a comparison circuit [[106]] for outputting ~~an incoincidence~~ a noncoincidence signal [[127]] in a case that the output data [[123]] of the memory [[101]] and the delay data [[124]] as compared are not coincident with each other ~~after compared~~.